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EXAMINER	
ROCHE, JOHN B	

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2184	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/687,786	LIEN ET AL.	
	Examiner	Art Unit	
	JOHN B. ROCHE	2184	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 July 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-9,11-15,17-22 and 24-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-9,11-15,17-22 and 24-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

2. Claims 1, 3-8 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harriman et al. (US 5,898,687), hereafter referred to as Harriman'687 in view of Turner et al. (US 7,106,693), hereafter referred to as Turner'693.

3. Referring to claim 1, Harriman'687 teaches a packet transmit queue control system comprising a first data structure embodied on a tangible computer readable medium (unicast output queue as seen in figure 3 and column 7, line 14) coupled to a packet controller (controller 254 as seen in figure 2 and column 7, line 12) and configured to store a plurality of first type packet pointers (each port of the switch has unicast output queue as seen in figure 3 and column 7, lines 13-14); a second data structure embodied on a tangible computer readable medium (multicast output queue as seen in figure 3 and column 7, line 14) coupled to the packet controller (controller 254 as seen in figure 2 and column 7, line 12) and configured to store a plurality of second type packet pointers (each port of the switch has multicast output queue as seen in figure 3 and column 7, lines 13-14), wherein the packet controller is configured to

receive a first sequence of packet pointers and to provide each packet pointer to one of the first and second data structures (controller 254 controls read pointers 256 and write pointers 258 to implement multicast queues 240 as seen in figure 2 and column 5, line 65 - column 6, line 2); and a port transmit controller coupled to the first and second data structures (round robin subarbiter circuits 332-338 as seen in figure 3 and column 7, line 30) and configured to provide a second sequence of packet pointers (RR subarbiters skew selection of the cell at each priority level, column 7, lines 31-32).

4. However, Harriman'687 does not teach the system wherein the first data structure includes a plurality of linked-list data structures.

5. Turner'693 teaches the system wherein the first data structure includes a plurality of linked-list data structures (multiple timing wheels as seen in figure 2A and column 6, lines 24-26; timing wheel implemented using a linked-list data structure 520 as seen in figure 5C and column 9, lines 3-5).

6. It would have been obvious to one of ordinary skill in the art at the time of invention to modify Harriman'687's system to incorporate, as taught by Turner'693, the method wherein the first data structure includes a plurality of linked-list data structures. The motivation to combine these teachings is to

effectively pace the flow of packets of information from networked devices (column 2, lines 3-4).

7. As to claim 3, Harriman'687 teaches the system of claim 1, wherein the second data structure includes a plurality of first-in first-out structures (dedicated multicast output queue for each output port of the switch at each priority level, column 2, lines 38-41).

8. As to claim 4, Harriman'687 teaches the system of claim 3, wherein each of the plurality of FIFO structures is coupled to a port (dedicated multicast output queue for each output port of the switch at each priority level, column 2, lines 38-41).

9. As to claim 5, Harriman'687 teaches the system of claim 1, wherein the first type packet pointers include unicast pointers (unicast output queue as seen in figure 3 and column 7, line 14); and the second type packet pointers include multicast pointers (multicast output queue as seen in figure 3 and column 7, line 14).

10. As to claim 6, Harriman'687 teaches the system of claim 1, wherein the second sequence of packet pointers includes post transmit scheduling information (data from queue occupancy calculation in SP component 320 determines priority as seen in figure 3 and column 7, lines 20-23).

11. As to claim 7, Harriman'687 teaches the system of claim 1, wherein an ordering of the second sequence of packet pointers is substantially consistent with a packet arrival order (at each cell time, arbitration mechanism 300 evaluates states of queue pairs, transmitting a cell from a non-empty pair having the highest priority as seen in figure 3 and column 7, lines 17-20).

12. As to claim 8, Harriman'687 teaches the system of claim 4, wherein the packet controller is configured to provide each of the plurality of second type packet pointers to each or a group of the plurality of FIFO structures (each port of the switch has multicast output queue as seen in figure 3 and column 7, lines 13-14; dedicated multicast output queue for each output port of the switch at each priority level, column 2, lines 38-41).

13. Turner'693 teaches the system of claim 4 wherein the packet controller is configured to provide each of the plurality of first type packet pointers to a selected one of the plurality of linked-list data structures (information stream identifier data structure pointer field 502 as seen in figure 5A and column 8, lines 49-50).

14. As to claim 32, Harriman'687 teaches the system of claim 1, wherein the port transmit controller is coupled to an output port (round robin subarbiter circuits 332-338 as seen in figure

3 and column 7, line 30; output port at each priority level, column 6, lines 31-33).

15. Claims 9 and 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harriman'687 in view of Turner'693 as applied to claims 1 and 3-8 above, and further in view of Hebb et al. (US 6,711,153), hereafter referred to as Hebb'153.

16. Referring to claim 9, Harriman'687 teaches a data arrangement for packet transmit queue control, comprising: a first data structure embodied on a tangible computer readable medium (unicast output queue as seen in figure 3 and column 7, line 14) configured to store a plurality of first type packet pointers (each port of the switch has unicast output queue as seen in figure 3 and column 7, lines 13-14); and a second data structure embodied on a tangible computer readable medium (multicast output queue as seen in figure 3 and column 7, line 14) configured to store a plurality of second type packet pointers (each port of the switch has multicast output queue as seen in figure 3 and column 7, lines 13-14).

17. Turner'693 teaches the data arrangement wherein the first data structure includes a linked-list structure (timing wheel implemented using a linked-list data structure 520 as seen in figure 5C and column 9, lines 3-5).

18. However, Harriman'687 and Turner'693 do not teach a third data structure embodied on a tangible computer readable medium coupled to the second data structure and configured to store a plurality of status flags.

19. Hebb'153 teaches a third data structure embodied on a tangible computer readable medium (control/status registers 80 as seen in figure 3) coupled to the second data structure (coupled to FIFOs 40 and 50 as seen in figure 3) and configured to store a plurality of status flags (status register configured to hold status information).

20. It would have been obvious to one of ordinary skill in the art at the time of invention to modify Harriman'687 and Turner'693's system to incorporate, as taught by Hebb'153, a third data structure embodied on a tangible computer readable medium coupled to the second data structure and configured to store a plurality of status flags. The motivation to combine these teachings is to facilitate performing quick and efficient route lookups (column 1, lines 34-36).

21. Claims 11-12 contain the corresponding limitations of claims 3 and 5, respectively; therefore, they are rejected using the same reasoning accordingly.

22. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Harriman'687, Turner'639 and Hebb'153 as applied to claim 9 above, and further in view of Chen et al. (US 6,958,973), hereafter referred to as Chen'973.

23. As to claim 13, Harriman'687 teaches the arrangement of claim 12, wherein each entry of the second data structure includes a packet pointer field (address pointer, column 2, line 19).

24. However, Harriman'687, Turner'639 and Hebb'153 do not teach the arrangement wherein each entry of the second data structure also includes a previous unicast pointer indication field; a next unicast pointer indication field; and a previous unicast pointer field.

25. Chen'973 teaches the arrangement wherein each entry of the second data structure also includes a previous unicast pointer indication field (unicast packet must be enqueued into port output queue preceding multicast packets, column 8, lines 6-8); a next unicast pointer indication field (input skip count register of port set into skip count field when next unicast packet is enqueued, column 8, lines 14-16); and a previous unicast pointer field (previous unicast packet location must be known in order to properly ascertain the number of multicast packets following said previous unicast packet).

26. It would have been obvious to one of ordinary skill in the art at the time of invention to modify Harriman'687, Turner'639 and Hebb'153's system to incorporate, as taught by Chen'973, the arrangement wherein each entry of the second data structure also includes a previous unicast pointer indication field; a next unicast pointer indication field; and a previous unicast pointer field. The motivation to combine these teachings is to provide an improved and simplified output queuing method for forwarding packets in sequence (column 5, lines 3-5).

27. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Harriman'687, Turner'693 and Hebb'153 as applied to claim 9 above, and further in view of Raza et al. (US 7,016,349), hereafter referred to as Raza'349.

28. As to claim 14, Harriman'687, Turner'693 and Hebb'153 do not teach the arrangement of claim 9, wherein the plurality of status flags includes a first type packet pointer head position indication; a first type packet pointer tail position indication; an overall head pointer indication; and an overall tail pointer indication.

29. Raza'349 teaches the arrangement of claim 9, wherein the plurality of status flags includes a first type packet pointer head position indication (UNICAST_HPTR as seen in figure 10 and

column 11, lines 14-15); a first type packet pointer tail position indication (tail pointer address as seen in figure 14 and column 14, lines 60-61); and an overall head pointer indication (UNICAST_HPTR and MULTICAST_HPTR as seen in figure 10 and column 11, lines 18-20).

30. While Harriman'687, Turner'693, Hebb'153 and Raza'349 teaches an overall tail pointer indication, said over tail pointer indication is simply an alternative arrangement in the art.

31. It would have been obvious to one of ordinary skill in the art at the time of invention to modify Harriman'687, Turner'693 and Hebb'153's system to incorporate, as taught by Raza'349, that the plurality of status flags includes a first type packet pointer head position indication; a first type packet pointer tail position indication; an overall head pointer indication; and an overall tail pointer indication. The motivation to combine these teachings is to enable an apparatus to extract in-band information or skip extraction and perform a look ahead operation (column 3, lines 13-17).

32. Claims 15, 17-21, 24-27 and 29-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harriman'687 and

Turner'693 as applied to claim 9 above, and further in view of Raza'349.

33. Referring to claim 21, Harriman'687 teaches (a) means determining if a pointer is a first type or a second type (generating a key over line 132 indicating whether a cell requires multicast replication as seen in figure 1 and column 4, lines 41-43); (b) if the pointer is the first type, means determining if an overall tail is the first type or the second type (generating a key over line 132 indicating whether a cell requires multicast replication as seen in figure 1 and column 4, lines 41-43); and (c) if the pointer is the second type, means for determining if the overall tail is the first type or the second type (generating a key over line 132 indicating whether a cell requires multicast replication as seen in figure 1 and column 4, lines 41-43). Also, Harriman'687 teaches the data structures embodied on a tangible computer readable medium (unicast output queue as seen in figure 3 and column 7, line 14).

34. Turner'639 teaches the method wherein the first data structure includes a plurality of linked-list data structures (multiple timing wheels as seen in figure 2A and column 6, lines 24-26; timing wheel implemented using a linked-list data structure 520 as seen in figure 5C and column 9, lines 3-5).

35. Raza'349 teaches (b) if the pointer is the first type and the overall tail is the second type, means for setting an overall tail flag to a first state (system 400 allowing a multicast queue to send to a single location and unicast queue to implement complex processing as seen in figure 13 and column 14, lines 27-29), and means for setting an entry to the first state (system 400 allowing a multicast queue to send to a single location and unicast queue to implement complex processing as seen in figure 13 and column 14, lines 27-29); means for getting a first type tail (tail pointer fetched from the FIFO pointer memory 134 as seen in figure 5 and column 7, lines 9-12); means for linking the pointer in a first data structure to the first type tail (address logic block 130 requests data from pointer memory 134 when a new queue address is requested as seen in figure 5 and column 7, lines 29-32); and means for setting the first type tail to the pointer (configuration logic 502 writes to queue pointer memory 504 as seen in figure 14 and column 15, lines 2-3); and (c) if the pointer is the second type and the overall tail is the second type, means for adding the pointer to a second data structure field with a second state (system 400 generates and stores multicast addresses as seen in figure 13 and column 14, lines 23-25); if the overall tail is the first type, means for adding the pointer to a field of a second data

structure with the first state (system 400 allowing a multicast queue to send to a single location and unicast queue to implement complex processing as seen in figure 13 and column 14, lines 27-29); and means for writing the overall tail flag to the second state (configuration logic 502 writes to queue pointer memory 504 as seen in figure 14 and column 15, lines 2-3).

36. Note that claim 15 contains the corresponding limitations of claim 21 as shown above; therefore, it is rejected using the same reasoning accordingly.

37. Claims 17 and 18 contain the corresponding limitations of claims 3 and 5 respectively as shown above; therefore, they are rejected using the same reasoning accordingly.

38. As to claim 19, Harriman'687 teaches the method of claim 15, wherein the first state includes a yes-state (RR subarbiter "1" state as seen in figure 3 and column 7, lines 45-46); and the second state includes a no-state (RR subarbiter "0" state as seen in figure 3 and column 7, line 48).

39. Note that claim 26 contains the corresponding limitations of claim 19 as shown above; therefore, it is rejected using the same reasoning accordingly.

40. As to claim 20, Raza'349 teaches the method of claim 15 wherein the first data structure is accessed at most once (system 600 performs write operation into main memory once every

eight cycles as seen in figure 15 and column 15, lines 58-60); and the second data structure is accessed at most once (system 600 performs write operation into main memory once every eight cycles as seen in figure 15 and column 15, lines 58-60).

41. Claims 24-27 contain the corresponding limitations of claims 3, 5 and 19-20 respectively as shown above; therefore, they are rejected using the same reasoning accordingly.

42. Claim 29 contains the corresponding limitations of claims 15 and 22 as shown elsewhere; therefore, it is rejected using the same reasoning accordingly.

43. Claims 30 and 31 contain the corresponding limitations of claims 9 and 1 respectively; therefore, they are rejected using the same reasoning accordingly.

44. Claim 33 contains corresponding limitations to claim 9 as shown above; therefore, it is rejected using the same reasoning accordingly.

45. Claims 22 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Raza'349 in view of Turner'693.

46. Referring to claim 22, Raza'349 teaches determining if an overall head is a first type (UNICAST_HPTR and MULTICAST_HPTR as seen in figure 10 and column 11, lines 18-20); if the overall head is the first type: getting a first type head (head pointer

fetched from storage element 134 as seen in figure 5 and column 7, lines 18-19); getting a first type pointer from a second data structure (UNICAST_HPTR may indicate the address of a head pointer of a unicast packet as seen in figure 10 and column 11, lines 38-40); determining if the first type head matches the first type pointer (READ_ADD_SYS and WRITE_ADD_SYS compared as seen in figure 19 and column 18, lines 53-54); and if a match, setting an overall head flag to a second state (FIRST_MC_HPTR may indicate the address of a head pointer for a multicast packet as seen in figure 10 and column 11, lines 44-45).

47. Turner'693 teaches updating the first type head with a next pointer from a first data structure (data structure 350 is updated to reflect new target time as seen in figure 3 and column 40-43).

48. Note that claim 28 contains the corresponding limitations of claim 22 as shown above; therefore, it is rejected using the same reasoning accordingly.

Response to Arguments

49. Applicant's arguments with respect to claims 1, 3-9, 11-15, 17-22 and 24-33 have been considered but are moot in view of the new ground(s) of rejection.

50. As to Applicant's arguments, Examiner believes that the revised grounds of rejection as shown above render said arguments moot.

51. As to Applicant's amendments of claims 1-14 and 21 to overcome the rejections under 35 U.S.C. 101 and 112, 2nd paragraph, Examiner agrees that said amendments overcome said rejections.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JOHN B. ROCHE whose telephone number is (571)270-1721. The examiner can normally be reached on 8:30 am - 5:00 pm, M-F EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Henry Tsai can be reached on 571-272-4176. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JR

/Henry W.H. Tsai/
Supervisory Patent Examiner, Art Unit 2184